What is claimed is:

1. A method of manufacturing a semiconductor device comprising:

sequentially forming a first semiconductor layer and a second semiconductor layer on a semiconductor substrate, wherein the second semiconductor layer has a lattice property different from the first semiconductor layer;

etching the second semiconductor layer and the first semiconductor layer to form a first semiconductor pattern;

forming a third semiconductor layer over the first semiconductor pattern, wherein the third semiconductor layer has a lattice property substantially the same as the lattice property of the first semiconductor layer; and

etching the third semiconductor layer to form a second semiconductor pattern covering the first semiconductor pattern.

2. The method of claim 1, wherein the first semiconductor layer comprises silicon and the second semiconductor layer comprises silicon-germanium.

3. The method of claim 2, wherein the second semiconductor layer is formed by an epitaxial growth process.

4. The method of claim 2, wherein the third semiconductor layer comprises silicon.

5. The method of claim 1, wherein the second semiconductor pattern

is formed on a top surface and on sidewalls of the first semiconductor pattern.

6. The method of claim 1, further comprising forming a gate on the second semiconductor pattern, the gate being substantially perpendicular to the first semiconductor pattern.

7. The method of claim 6, wherein a gate oxide layer is formed between the gate and the second semiconductor pattern.

8. The method of claim 6, comprising forming a metal silicide layer on a top surface of the gate.

9. A method of claim 1, comprising injecting impurities in the first semiconductor pattern and in the second semiconductor pattern.

10. A semiconductor device comprising a transistor channel, wherein:
the channel comprises an inner portion and an outer portion;
the outer portion surrounds the inner portion; and
the inner portion and the outer portion have different lattice properties.

11. The apparatus of claim 10, wherein the inner portion comprises silicon-germanium and the outer portion comprises silicon.

12. The apparatus of claim 10, wherein the outer portion surrounds the inner portion on at least three sides.

13. The apparatus of claim 10, comprising a gate formed over the channel.

14. The apparatus of claim 13, wherein the gate is substantially perpendicular to the channel.

15. The apparatus of claim 13, wherein the gate surrounds at least a section of the channel on at least three sides.

16. The apparatus of claim 13, wherein a gate oxide is formed between the channel and the gate.

17. The apparatus of claim 13, wherein a metal silicide layer is formed on a top surface of the gate.

18. The apparatus of claim 10, wherein the thickness of the inner portion is between 10 nm and 90 nm.

19. The apparatus of claim 10, wherein the thickness of the outer portion is between 10 nm and 100 nm.

20. The apparatus of claim 10, wherein the outer portion includes a layer is formed between the inner portion and the semiconductor substrate.

21. The apparatus of claim 20, wherein the layer comprises silicon.

22. The apparatus of claim 21, wherein the layer is strained silicon.

23. The apparatus of claim 20, wherein the layer comprises approximately the same lattice property as the outer portion.

24. The apparatus of claim 20, wherein the thickness of the layer is between 10 nm and 30 nm.

25. The apparatus of claim 20, wherein:

the semiconductor substrate comprises a source region and a drain region; and

the channel is coupled to the source region and the drain region.